AMENDMENTS TO THE CLAIMS

1-5. (Canceled)

6. (Currently amended) A method for fabricating a CMOS image sensor, comprising:

a) providing a semiconductor structure, wherein the semiconductor structure includes an impurity region and a gate electrode;

b) forming a first spacer on a first sidewall of the gate electrode and a fourth spacer on a second side wall of the gate electrode, wherein the first spacer is overlapped with a portion of the impurity region; [[and]]

c) removing the fourth spacer by a photo resist pattern covering the impurity region and the first spacer; [[and]]

d) forming a second spacer on a sidewall of the first spacer and a third spacer on a second sidewall of the gate electrode after removing the fourth spacer;

e) carrying an ion implantation to form a P-type impurity region on the impurity region to thereby obtain a photodiode; and

f) forming a floating diffusion region spaced away from the impurity region by a predetermined distance.

7. (Original) The method as recited in claim 6, comprising:

b1) forming a first oxide layer on the semiconductor structure; and

b2) carrying out an etching process to form the first spacer.

8. (Original) The method as recited in claim 7, comprising forming the first oxide layer by carrying out a thermal oxidation process.

9. (Canceled)

10. (Previously presented) The method as recited in claim 7, comprising:

c1) forming a photoresist pattern covering the impurity region and the first spacer;

c2) carrying out an etching process to remove the fourth spacer;

c3) removing the photoresist pattern;

c4) forming a second oxide layer on a resulting substrate; and

c5) carrying out an etching process to form the second spacer and the third spacer.

11. (Original) The method as recited in claim 10, comprising forming the second oxide layer by carrying out a thermal oxidation process.

12 – 18. (Canceled)

19. (New) A method for fabricating a CMOS image sensor, comprising:

providing a semiconductor structure, wherein the semiconductor structure includes an impurity region and a gate electrode;

forming a first spacer pair on both sidewalls of the gate electrode, wherein one spacer of the first spacer pair is overlapped with a portion of the impurity region;

removing the other spacer of the first spacer pair by a photo resist pattern covering the impurity region and the one spacer of the first spacer pair; and

forming a second spacer pair on both sidewalls of the first spacer and the gate electrode after removing the other spacer of the first spacer pair.

20. (New) The method as recited in claim 19, wherein the providing the semiconductor structure comprises

forming a first oxide layer on the semiconductor structure; and

carrying out an etching process to form the first spacer pair.

21. (New) The method as recited in claim 20, wherein the first oxide layer is formed by carrying out a thermal oxidation process.

22. (New) The method as recited in claim 19, wherein the removing the other spacer of the first spacer pair comprises

c1) forming a photoresist pattern covering the impurity region and the one spacer of the first spacer pair;

c2) carrying out an etching process to remove the other spacer of the first spacer pair;

c3) removing the photoresist pattern;

c4) forming a second oxide layer on a resulting substrate; and

c5) carrying out an etching process to form the second spacer pair.

23. (New) The method as recited in claim 22, wherein the second oxide layer is formed by carrying out a thermal oxidation process.

24. (New) The method as recited in claim 19, wherein the impurity region is an N-type.

25. (New) The method as recited in claim 24, further comprising:

carrying an ion implantation to form a P-type impurity region on the impurity region to thereby obtain a photodiode; and

forming a floating diffusion region spaced away from the impurity region by a predetermined distance.

26. (New) The method as recited in claim 19, wherein the first spacer pair has different width with the second spacer pair.